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The following is an extract relevant to the present application.

A method of square root extraction computation including:

a first step wherein a content A of a first resistor in which a number to be square-root extracted is set is shifted in to a second resistor by two digits from the most significant digit;

a second step wherein a content B of said second resistor and a content C of a third resistor in which 1 is set as the least significant digit are compared; and

a third step wherein when  $B \geq C$ , (B-C) is set to said second resistor and (C+1) is set to said third resistor and when  $B < C$ , said content C of said third resistor is reduced by 1,

wherein when said first to third steps have not been repeated predetermined times, said content C of said third resistor is shifted to an upper digit by one digit and 0 is set as the least significant digit and then said first to third steps are repeated; and

wherein when said first to third steps have been repeated predetermined times it is so arranged that said third resistor generates a computation result which is double the square root extraction result.





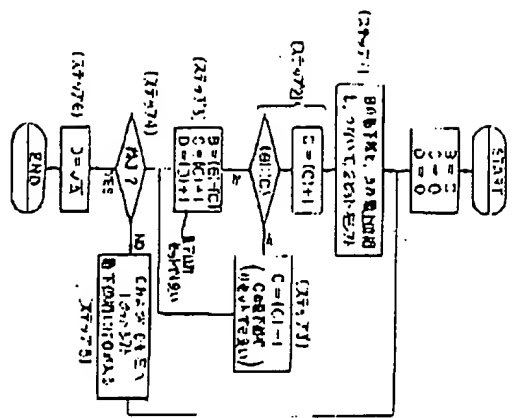




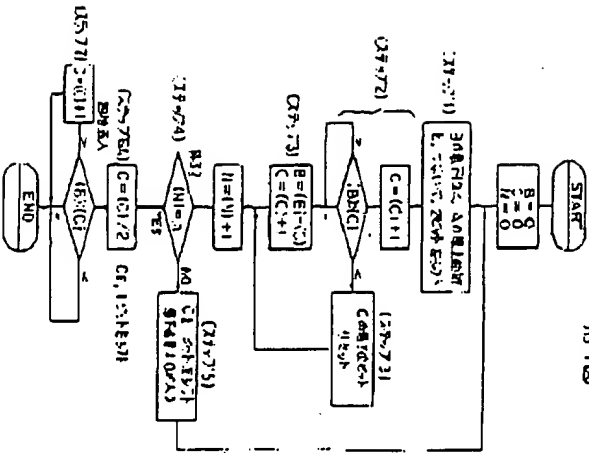
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第3 图



第4 图



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